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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/869,274	06/26/2001	Asao Nishimura	H 987	2371

24956 7590 08/29/2003

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SUITE 370
ALEXANDRIA, VA 22314

EXAMINER

COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 08/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/869,274	Applicant(s) NISHIMURA ET AL.	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 13 June 2003.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-9 and 23-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-9 and 23-28 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Response to Arguments

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 3, 9, 23, 24, 25, 26, 27 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Strauss U.S. Patent 5,719,449.

4. Pertaining to claim 1, Strauss teaches a semiconductor device as claimed. See **FIGS. 1-4** where Strauss discloses a semiconductor integrated circuit device comprising:

a semiconductor substrate **201**; a plurality of circuit elements (shown in fig. 1) formed in an element forming layer on said semiconductor substrate;

a plurality of first and second terminals **222, 224** formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a plurality of conductive **217** layers which are respectively connected to said first terminals corresponding to some terminals of said plurality of terminals and extending on said element forming layer;

protruding electrodes **225** (solder bumps) respectively connected to said conductive layers;

testing pads **222, 223** respectively connected to said second terminals, said testing pads being not coupled to any protruding electrode; and

an insulating film **219, 220 and 221** which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

5. Pertaining to claim 2, Strauss teaches a semiconductor device as claimed. See **FIG. 2** where Strauss teaches a semiconductor integrated circuit device comprising: a semiconductor substrate; a plurality of circuit elements formed in an element forming layer on said semiconductor substrate; first and second terminals formed on the surface of said element forming layer and connected to predetermined ones said circuit elements;

conductive layer which is connected to first terminal;

protruding electrode connected to
said conductive layer;

a testing pad connected to said second terminal, said testing pad being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrode and said testing pad so as to expose said protruding electrodes and said testing pad.

6. Pertaining to claim 3, Strauss teaches the semiconductor integrated circuit device according to claim 1, wherein said conductive layers are metal wirings, said insulating film is formed on said each metal wiring, and an insulating film is further formed below said each metal wiring.

7. Pertaining to claim 9, Strauss teaches the semiconductor integrated circuit device according to claim 1, wherein said testing pads extend on said further insulating film.

8. Pertaining to claim 23, Strauss discloses a semiconductor integrated circuit device comprising: a semiconductor substrate; a first circuit element and a second circuit element formed on said semiconductor substrate;
a wiring formed over said semiconductor substrate and connected to said first circuit element;
a bump formed over said wiring and connected thereto; and
a conductive layer, which is formed over said semiconductor substrate and connected to said second circuit element and which constitutes a testing pad, wherein said conductive layer is electrically isolated from any bump.

9. Pertaining to claim 24, Strauss teaches a semiconductor integrated circuit device comprising: a semiconductor substrate;

a semiconductor integrated circuit element formed in said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said semiconductor integrated circuit element;

a bump formed on said wiring and connected thereto; and a conductive layer, which is formed on said semiconductor substrate and connected to said semiconductor integrated circuit element and which constitutes a testing pad which is electrically isolated from any bump, wherein when said semiconductor integrated circuit element is tested, said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and when said semiconductor integrated circuit element is in normal operation, said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

10. Pertaining to claim 26, Strauss discloses a semiconductor integrated circuit device comprising: a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said first circuit element;

a bump formed on said wiring and connected thereto;

a first conductive material, which is formed on said semiconductor substrate and connected to said first circuit element and which constitutes a first testing pad; and

a second conductive material, which is formed on said semiconductor substrate and connected to said second circuit element and which constitutes a second testing pad which is not connected to any bump, wherein when said first circuit element and said second circuit element are tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device, and when said first circuit element and said second

Art Unit: 2823

circuit element are in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device through said bump, and said second testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

11. Pertaining to claim 27, Strauss teaches a semiconductor integrated circuit device comprising: a semiconductor substrate; an integrated circuit formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said integrated circuit; a bump formed on said wiring and connected thereto;

a first conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a first testing pad; and

a second conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a second testing pad which is not connected to any bump,

wherein said first conductive layer and said wiring are connected to each other, and when said integrated circuit is tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device and when said integrated circuit is in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device and said second testing pad is electrically isolated from the outside of said semiconductor integrated circuit device.

12. Pertaining to claim 25, Strauss teaches a semiconductor integrated circuit device comprising:

Art Unit: 2823

a semiconductor substrate;
integrated circuit elements formed on said semiconductor substrate;
a plurality of wirings formed on said semiconductor substrate and connected to said integrated circuit elements;
a plurality of bumps formed on said plurality of wirings and provided in association with said plurality of wirings;
a conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit elements and which is formed as a testing pad which is electrically isolated from any bump; and
an organic film placed on said semiconductor substrate and formed below said plurality of wirings, wherein when each said integrated circuit element is tested, said each testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and when each said integrated circuit element is in normal operation, each said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

13. Pertaining to claim 28, Strauss teaches a semiconductor integrated circuit device comprising:

a semiconductor substrate;
integrated circuit elements formed on said semiconductor substrate;
a plurality of wirings formed over said semiconductor substrate and connected to at least one of said integrated circuit elements;

a plurality of bumps formed over said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed over said semiconductor substrate and connected to at least one of said integrated circuit elements and which constitutes a test pad which is not connected to any bump; and

a film containing an organic material formed between said semiconductor substrate and said plurality of wirings and between said semiconductor substrate and said conductive layer, wherein when said integrated circuit element is tested, said test pad is electrically connected to the outside of said semiconductor integrated circuit device, and when said integrated circuit element is in normal operation, said test pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 4, 5, 6, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

— Strauss, U.S. Patent 5,719,449 as applied to claims 1, 2, 3, 9, 23, 24, 26 and 27 above, and further
in view of Iwabuchi, U.S. Patent 6,030,890.

16. Pertaining to claims 4 and 5, Strauss discloses a semiconductor device substantially as claimed. However, Strauss fails to teach the semiconductor integrated circuit device according to claim 3, wherein said insulating film and said further insulating film are respectively formed different materials, and said insulating film is formed of a material higher in elastic modulus than said further insulating film. See **FIG. 3B**, where Iwabuchi teaches wherein said insulating film and said further insulating film are respectively formed different materials, and said insulating film is formed of a material higher in elastic modulus than said further insulating film. In view of Iwabuchi, it would have been obvious to one of ordinary skill in the art to incorporate said insulating film having a material higher in elastic modulus than said further insulating film because the first interlayer insulator is a spin-coated layer (column 6, lines 46-55). Please note that any spin-on coating which has a solvent that requires it to be driven off is an organic substance.

17. Pertaining to claim 6, Strauss fails to teach the semiconductor integrated circuit device according to claim 5, wherein the film containing the organic substance is a polyimide film, a fluorocarbon resin film, or an elastomer film which contains a silicon or acrylic rubber material. Iwabuchi teaches wherein the film contains a polyimide film. In view of Iwabuchi, it would have been obvious to one of ordinary skill in the art to incorporate a polyimide film into the Strauss semiconductor device because the polyimide is a spin-coated layer (column 6, lines 45-55).

18. Pertaining to claim 7, Strauss discloses the semiconductor integrated circuit device according to 1, wherein said testing pads are placed

Art Unit: 2823

just above said terminals corresponding thereto.

19. Pertaining to claim 8, Strauss teaches the semiconductor integrated circuit device according to claim 7, wherein said testing pads are regularly placed in the central portion of said semiconductor substrate, and said protruding electrodes are regularly placed outside said testing pads respectively.

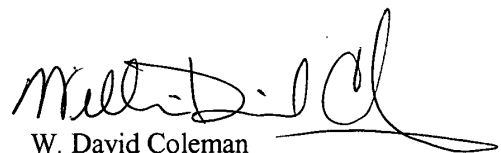
Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004.

The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC
June 23, 2003